Dr. ENVER ÇAVUŞ
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EDUCATION

University of California Los Angeles (UCLA), School of Engineering
PhD in Electrical Engineering
Dissertation Title: "Techniques for the Decoding of LDPC Codes: Efficient Simulation, Algorithm Improvement and Implementation"
University of California Los Angeles (UCLA), School of Engineering
Master of Science in Electrical Engineering
Dissertation Title: "A Computationally Efficient ASIC Implementation of Space-Time Block Decoder"
University of Southern California (USC), School of Engineering
Bachelor of Science in Electrical Engineering

WORK EXPERIENCE

Associate Professor, Ankara Yıldırım Beyazıt University, (04/12-Present).
- Digital Signal Processing, VLSI implementation of Communication Systems, Error Correction Coding, High-Performance Computing

Co-Founder, Tera-Hz Microelectronics, Ankara, Turkey (08/2012 - Present).
- CMOS VLSI, analog, mixed signal and RF design ranging from product definition to development.
- System Modeling, Performance Analysis, and FPGA/ASIC implementation of Low Density Parity Check Codes forward error correcting (FEC) schemes intended for the 10GBase-T Ethernet (IEEE 802.3an), G.hn/G.9960 (ITU-T Standard for networking over power lines, phone lines and coaxial cable), DVB-S2 (Digital video broadcasting second generation), WiMAX (IEEE 802.16e standard for microwave communications), IEEE 802.11n (Wireless Local Area Network) and, WiGig Standard (Wireless Gigabit Communication over the unlicensed 60GHz Band).

Staff Scientist, Broadcom Corporation, Irvine, CA (09/06-09/09).
- ASIC prototyping of DVB-S2, DVB-T2, CMMB, and 10Gb Ethernet systems with Xilinx-IV FPGAs. Implemented many communication blocks including MPEG Packetizer, adaptive multi-rate BCH and LDPC Codecs, QPSK-32APSK Modulator/Demodulator, Digital Noise Generator, and BERT modules.
- Design automation of RTL generation, simulation, synthesis, place and route, and verification steps using perl scripts. Modelled generic verilog FIFO, Memory and Interleaver/Deinterleaver blocks for different applications.
- Synthesis, timing closure and test vector generation of BCH and LDPC cores in multiple Single Chip Advanced Satellite Set Top Box SoC projects.
- Low BER performance analysis of LDPC codes and evaluation of alternative decoding algorithms.

Design Engineer, Silvus Communications Systems Inc., Los Angeles, CA (03/05-09/05).
- Simulation and architecture definition for a high throughput multi-rate LDPC codec for IEEE 802.11n standards.
- DDC implementation using Xilinx Virtex-II FPGAs.

Intern, IBM T. J. Watson Research Center, Yorktown Heights, NY (05/04-12/04).
- Developed novel techniques for the performance evaluation of LDPC Codes at low BERs.
- Designed a fully parallel LDPC decoder in VHDL for an FPGA implementation.

Graduate Research Assistant, Wireless Integrated Systems Research Lab, UCLA, (09/99-03/07).
- Efficient implementation of rate compatible LDPC codes for low BER applications.
- Developed unique techniques to improve performance and decoding complexity of LDPC codes.
- A very low complexity ASIC implementation for decoding of Space-Time Block Codes (STBCs)

Intern, Applied Micro Circuits Company (AMCC), San Diego, CA (05/98-08/98).
- Debugging, determining specs for new products and analyzing the results.

PROJECTS

- **Principal Investigator**, Development of Microbolometer Integrated Circuit Employing VCO-Based ADC, TUBITAK 1001, (12/18-12/20).
- **Principal Investigator,** An Experimental Channel Coded MIMO-OFDM Communication System at 0.24 THz for NLOS Indoor Applications, TUBITAK 1001, (09/15-03/18).
- **Researcher,** Distributed Sensor and Communication Network with GPS in ISM band, TUBITAK 1511, (03/17-03/19).
- **Principal Investigator,** Development of High Performance IP Cores for Low Density Parity Check Codes, TUBITAK 1511, (05/13-05/15).
- **Principal Investigator**, Design and Development of High Speed Hardware Architectures, TUBITAK UZAY, 02/15-02/16).
- **Principal Investigator**, Analysis of Efficient Coding Techniques Against Multi-Bit Upset Errors of SRAM Based Devices, AYBU BAP, (02/14-02/16).
- **Researcher,** Efficient ASIC Implementation of Space-Time Block Decoder, DARPA, (09/00-06/02).

THESIS SUPERVISED

- "Study of Utilizing Multiple Inertial Measurement Units for Strapdown Inertial Navigation Systems without GPS Aid", Osman Tokluoglu, AYBU, 2019.
- "An Optimized FFT based Acquisition Method for GPS Receivers", Nejat Yenigün, AYBU, 2019.
- "Performance Comparison of Image Matching Algorithms using FPGA and GPU", İrfan Alp Gürkaynak, AYBU, 2017.
- "An Efficient FPGA Implementation of a Soft Decision Demapper for Digital Communication Systems", Emre Kırkaya (Co-Advisor), 2016.
- "Syndrome Array Decoding of EG-LDPC Based 2-Dimensional Error Correcting Codes for Mitigating MBUs of SRAM Memories" Ahmet Turan Erozan, AYBU, 2015.
- "Performance Improvement Methods for Layered Decoding of LDPC Codes" Murat Sever, YBU, 2015.
- "Design and Implementation of a 2 – 18 GHz RF Downconverter using Adjustable Filters for EW Applications" Bekir Şentürk, GYTE, 2014.
- "2-Dimensional EG-LDPC Codes for Achieving Fault Tolerance in SRAM Based Devices", Mustafa Demirci (Co-Advisor), TOBB ETÜ, 2013.
- "The Design of a Linux Based, 3G Capable Modbus Gateway System With Intelligent Modbus Message Prioritization Mechanism For Industrial Applications", Beşir Demir, GYTE, 2012.
- "Analysis and Implementation of Lorenz Chaotic System using Fixed Point Modelling on FPGA", Emre Güngör, Bilecik University, 2012.
- "Improving Classroom Interaction through SMS and Android Based Applications", Yusuf Muştu, Bilecik University, 2012.

PATENTS

- Tekin, A. Emira, S. Ay, E. Çavuş, A. Mohieldin, "Traveling Wave Based High-Speed Sampling Methods," US Patent # 9,191,020 B2, November 2015.

PUBLICATIONS

- Serdar Özyurt, Mustafa Öztürk, Enver Çavuş, "Low Complexity MIMO MMSE Receiver with Performance Enhancement via Coordinate Interleaving", Journal of Circuits, Systems, and Computers (JCSC), 2020.
- A. Çağlan, A. Çiçek, E. Çavuş, E. Bedeer, H. Yanikomeroglu "Polar Coded Faster-than-Nyquist (FTN) Signaling with Symbol-by-Symbol Detection", IEEE Wireless Communications and Networking Conference (WCNC), 2020.
- M. A. Gülden, E. Zencir, E. Çavuş, "A Novel Current Controlled Oscillator Based Low Supply Voltage Microbolometer Readout Architecture", Journal of Circuits, Systems, and Computers (JCSC), 2019.
- M. A. Reşat, A. Çiçek, S. Özyurt, E. Çavuş, "Analysis and FPGA Implementation of Zero-Forcing Receive Beamforming with Signal Space Diversity under Different Interleaving Techniques", Journal of Circuits, Systems, and Computers (JCSC), 2019.
- O. Tokluoglu, E. Çavuş, "Study of Utilizing Multiple IMUs for Inertial Navigation Systems Without GPS Aid", 1st Global Power, Energy and Communication Conference (GPECOM), 2019.
- M. C. Karakoç, M. F. Sertkaya, E. Kırkaya, E. Çavuş, "FPGA Implementation of Synchronization Techniques used in OFDM Systems", 27th IEEE Signal Processing and Communications Applications Conf., 2019.
- B. Demir, A. Tümay, M. Efe Özbek, E. Çavuş, "Design of a System Solution That Modernizes Legacy SCADA Systems as an Early Detection System", Transactions of the Institute of Measurement and Control, Vol 51, Issue 7-8, 2018.
- M. Öztürk, E. Kırkaya, E. Balcısoy, M. Şanlı, A. Çiçek, Enver Çavuş, "Baseband Implementation of High Speed Communication System on FPGA", 26th IEEE Signal Processing and Communications Applications *Conf*., 2018.
- M. Şanlı, M. Öztürk, E. Balcısoy, M. C. Karakoç, E. Kırkaya, A. Çiçek, S. Özyurt, E. Çavuş, "FPGA Implementation of MMSE Channel Estimation Algorithm Using System Generator", *26th IEEE Signal Processing and Communications Applications Conf*., 2018.
- M. C. Karakoç, M. A. Gülden, E. Kırkaya, Ö. Ersoy, M. Şanlı, A. Çiçek, E. Çavuş, S. Özyurt,"FPGA Implementation of Symbol Timing Synchronization for OFDM Systems", *26th IEEE Signal Processing and Communications Applications Conf*., 2018.
- E. İnceöz, E. Çavuş, "FPGA Implementation of Variable-Length Split-Radix FFT Algorithm", *International Journal of Engineering Science and Computing*, 2017.
- Ö. Ersoy, A. B. Şahin, A. Çiçek, M. C. Karakoç, E. Çavuş, S. Özyurt "Design of Frequency Upconversion and Downconversion Blocks for 240 GHz Communication Systems", *25th IEEE Signal Processing and Communications Applications Conf.*, 2017.
- A. Çağlan, E. Balcısoy, E. Kırkaya, G. Charyyev, A. Çiçek ve E. Çavuş, "FPGA Implementation of Layered Low Density Parity Check Error Correction Codes", *25th IEEE Signal Processing and Communications Applications Conference*, 2017.
- M. Sever, E. Çavuş, "Parallelizing LDPC Decoding using OpenMP on Multicore Digital Signal Processors", *The International Workshop on Embedded Multicore Systems (ICPP-EMS)*, 2016.
- A. Çağlan, E. İnceöz, E. Balcısoy, M. E. Özbek, E. Çavuş, "FPGA Implementation of AWGN Noise Generator Using Box-Muller Method", *24th IEEE Signal Processing and Communications Applications Conference*, 2016.
- A. T. Erozan, E. Çavuş, "An EG-LDPC Based 2-Dimensional Error Correcting Code for Mitigating MBUs of SRAM Memories", *FPGA World Conference*, 2015.

- M. Sever, E. Çavuş, “A Simple Adaptive Scheduling Technique for Decoding of LDPC Codes”, *IET Electronics Letters*, Vol. 51, no. 16, p. 1261 - 1263, 2015.
- E. Çavuş, C. Haymes, B. Daneshrad, “Low BER Performance Estimation of LDPC Codes via Application of Importance Sampling to Trapping Sets”, *the IEEE Transactions on Communications,* July 2009.
- E. Çavuş, B. Daneshrad, “Computationally Efficient Decoding of LDPC Codes”, *Electronics Letters*, vol. 45, no. 18, pp. 946-948, 2009.
- E. Çavuş, C. Haymes, B. Daneshrad, “An IS Simulation Technique for Very Low BER Performance Evaluation of LDPC Codes”, *Proceedings of the IEEE International Communications Conference* (ICC), Istanbul, Turkey, June 2006.
- E. Çavuş, B. Daneshrad, “A Very Low Complexity Space-Time Block Decoder (STBD) ASIC for Wireless Systems" *the IEEE Transactions on Circuits and Systems I*, vol. 53, no. 1, pp. 60-69, 2006.
- E. Çavuş, B. Daneshrad, “A Performance Improvement and Error Floor Avoidance Technique for Belief Propagation Decoding of LDPC Codes" *Proceedings of IEEE International Symposium on Personal Indoor and Mobile Radio Communications (PIMRC),* Berlin, Germany, 2005.
- E. Çavuş, B. Daneshrad, “A Computationally Efficient Selective Node Updating Scheme for Decoding of LDPC Codes" *Proceedings of IEEE Military Communication Conference (MILCOM),* New Jersey, 2005.
- E. Çavuş, B. Daneshrad, “A Computationally Efficient Algorithm for Space-Time Block Decoding” *Proceedings of IEEE International Communications Conference* (ICC), Helsinki, Finland, 2001.

HONORS AND AWARDS

- *First place (Best Overall) at 2003 DAC/ISSCC Student Design Contest* (Operational Category) for the “A Computationally Efficient ASIC Implementation for the Decoding of Space-Time Block Codes”.
- *Ranked 75th among 1.3 million* students in National University Entrance Exam, Turkey. (1994).
- *Full scholarship recipient* for a B.Sc. degree in the US awarded by Turkish Ministry of Education. (1994).
- *High scholastic achievement* award by Phi Kappa Phi Honor Society, USC. (Fall 97).
- *Member of TAU BETA PI and Golden Key* National Engineering Honor Societies. (02/98-Present).

COMPUTER SKILLS

Programming Languages: C, C++, Matlab, Perl, Tcl.
Engineering Applications: VHDL, Verilog, Vivado, Synopsys Design Compiler, PrimeTime, Certify, Virtuoso Layout Editor, Silicon Ensemble, Calibre, Spice.